

App. Serial No.: 10/801,942

Atty. Docket No.: 0057-011

### REMARKS

These remarks are in response to the Office Action dated January 29, 2007, which has a shortened statutory period for response set to expire April 29, 2007. A one-month extension, to expire May 29, 2007, is requested in a petition filed herewith.

#### Claims

Claims 1-44 are pending in the above-identified application. Claims 1-44 are rejected over prior art. Claims 1, 3-4, 7-8, 11-14, 17, 19, 23, 29, 35, and 40-43 are amended and Claims 45-59 are added. Claims 27, 28, and 39 are canceled. Claims 2, 5-6, 9-10, 15-16, 18, 20-22, 24-26, 30-34, 36-38, and 44 remain as originally filed or previously presented. Reconsideration is requested.

#### Claim Objections

Claim 1 is objected to due to a redundant occurrence of the term "and." Claim 1 is amended herein to delete the second occurrence of the term "and." Withdrawal of the objection is respectfully requested.

#### Rejections Under 35 U.S.C. § 112

Claims 40-41 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner writes: "In particular, the terms "substantially the same" and "mirror image" are indefinite."

Claim 40 is amended herein to delete the term "substantially." Applicant respectfully asserts that Claim 40 now satisfies the requirements of 35 U.S.C. §112, second paragraph.

Claim 41, is amended herein for clarity. Claim 41 now recites that a first one of the computers is directly adjacent a second one of the computers and that the first one of the computers is a mirror image of the second one of the computers.

In addition, Applicant points out that the term "mirror image" has a well defined meaning. For example, Merriam-Webster Online Dictionary defines "mirror image" as "something that has its parts reversely arranged in comparison with another similar thing or that is reversed with reference to an intervening axis or plane." Because the term "mirror image" has

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a well defined meaning, withdrawal of the rejection of Claim 41 under 35 U.S.C. § 112 is respectfully requested.

For the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 112.

#### Rejections Under 35 U.S.C. § 102

Claims 1-4, 6-7, and 12-13 are rejected under 35 U.S.C. § 102 (b) as being anticipated by U.S. Publication No. 2003/0028750 (Hogenauer). Applicant appreciates the Examiner's clear statement of his interpretation of the previous limitation "hard wired."

Claim 1 is amended herein to overcome the rejections under 35 U.S.C. § 102. In particular, Claim 1 now recites (in part): "the data paths being dedicated for communication between associated pairs of the computers." As indicated in Applicant's previous response, Hogenauer does not disclose dedicated interconnections between the computers. For this reason, Applicant respectfully requests withdrawal of the rejection of Claim 1 under 35 U.S.C. § 102. Claims 2-4, 6-7, and 12-13 depend from Claim 1 and are, therefore, distinguished from the cited reference for at least the same reasons as Claim 1.

#### Rejections Under 35 U.S.C. § 103

Claims 1-4, 6-7, 12-14, 17-21, 23-28, 34, 40-41, and 43 are rejected under 35 U.S.C. § 103 as being unpatentable over Hogenauer in view of U.S. Patent No. 6,460,128 (Baxter). The Examiner writes:

Hogenauer fails to disclose dedicated wiring exclusively between two computers of the array.

Baxter discloses transfer of information between nodes through a dedicated bus (col 3 lines 34-38).

As described in col 3 lines 34-38, Hogenauer would have been motivated to utilize this technique to avoid bus contention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hogenauer and allow processing nodes to communicate through dedicated lines as supported by Baxter.

Applicant respectfully traverses.

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M.P.E.P. § 2142 sets forth the procedural framework for the examination process of determining obviousness:

The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness. If, however, the examiner does produce a *prima facie* case, the burden of coming forward with evidence or arguments shifts to the applicant who may submit additional evidence of nonobviousness...

M.P.E.P. §2143 sets forth the requirements of a *prima facie* case of obviousness:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Thus, if any element of the *prima facie* case of obviousness is not met, the obviousness rejection is improper and should be withdrawn.

Claims 1-4, 6-7, 12-13, 34, and 40-41:

As amended herein, Claim 1 now recites:

1. A computer array, comprising:  
a plurality of computers integrated on a unitary substrate; and  
a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of the computers; and wherein,  
at least some of the computers are assigned a task different from that assigned to the other computers.

The combination of Hogenauer and Baxter is improper, because there is no suggestion to combine the references. Therefore, the first element of the *prima facie* case of obviousness is not satisfied.

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As the Examiner correctly asserts, Baxter discloses using dedicated busses to interconnect a network of computers each mounted on an adapter card to reduce buss contention. However, there is no indication in Hogenauer that bus contention is a problem in the adaptive computer engine. Nor is there any indication in Baxter that dedicated interconnections would be advantageous in an array of computers integrated on a unitary substrate.

Providing dedicated data lines would be unworkable in the architecture of Hogenauer. In particular, each of the matrices 150 is controlled by matrix controller 130 of controller 120, which is a RISC processor (para. 0015). Thus, controller 120 must necessarily be connected to each of the (N) matrices 150. Connecting all (N) of the matrices 150 to controller 120 with dedicated lines would require that an impractical number of interconnection lines be connected to controller 120. For example, for a 32-bit system, 32 times N lines would be required just to transmit data. Of course additional lines would be required for timing and control. Having to provide so many data lines would be a tremendous disadvantage, especially in an integrated circuit chip where chip "real estate" is so expensive, and especially where there is no indication that bus contention is a problem.

In addition to the data lines between controller 120 and matrices 150, data lines would be required between individual matrices 150, because Hogenauer indicates that the matrices 150 can be interconnected through the matrix interconnection network 110 (para. 0016). Interconnecting each of the matrices to each of the other matrices would require  $(N-1) + (N-2) + (N-3) + \dots + 1$  sets of connecting lines. To interconnect only ten matrices would require 45 additional sets of 32 data lines just to communicate data between all of matrices 150.

Furthermore, as indicated above, matrices 150 of Hogenauer are controlled by a single controller 120, which can only communicate with one of the matrices at a time, and so would only use one set of data lines at a time. Therefore, extra dedicated data lines would provide no useful purpose. Thus, there would be no motivation to introduce the unnecessary complexity in fabrication and design to provide data lines that serve no useful purpose.

For the foregoing reasons, Applicant respectfully asserts that there is no suggestion or motivation in the prior art to modify the adaptive computing engine of Hogenauer with the dedicated busses of Baxter. Therefore, no *prima facie* case of obviousness is established with respect to Claim 1. Reconsideration and withdrawal of the rejection of Claim 1 is respectfully

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requested. Claims 2-4, 6-7, 12-13, 34, and 40-41 depend, either directly or indirectly from Claim 1 and are, therefore, distinguished from the prior art for at least the same reasons as Claim 1.

Furthermore, Applicant objects that the combination of Hogenauer and Baxter is improper, because Baxter is non-analogous art. The two part test for determining whether prior art is analogous is as follows:

Two criteria are relevant in determining whether prior art is analogous: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the art is not within the same field of endeavor, whether it is still reasonably pertinent to the particular problem to be solved. *Wang Laboratories v. Toshiba*, 993 F.2d 858, 26 USPQ 2d 1767 (Fed. Cir. 1993).

In the *Wang Laboratories* case, the inventions related to single in-line memory modules (SIMMs) packaged in plastic leaded chip carriers (PLCCs). The questionable prior art related to (SIMMs) packaged in ceramic dual in-line packages (ceramic DIPs). With respect to whether the Allen-Bradley reference was within the inventor's field of endeavor, the Court stated:

The Allen-Bradley art is not in the same *field of endeavor* as the claimed subject matter merely because it relates to memories. It involves memory circuits in which modules of varying sizes may be added or replaced; in contrast, the subject patents teach compact modular memories. *Id.* (emphasis added)

In determining whether the Allen-Bradley art was reasonably pertinent to the particular problem the inventor attempted to solve, the Court stated:

Wang's SIMMs were designed to provide compact computer memory with minimum size, low cost, easy repairability, and easy expandability. ... In contrast, the Allen-Bradley patent relates to a memory circuit for a larger, more costly industrial controller ... Thus, there is substantial evidence in the record to support a finding that the Allen-Bradley prior art is not *reasonably pertinent* and is not analogous. (emphasis added)

The obviousness rejection of Claim 1 over Baxter is remarkably similar to the facts of the *Wang Laboratories* case. As recited in Claim 1 Applicant's field of endeavor is computer arrays integrated in unitary substrates. Baxter deals with connecting computers mounted on adapter cards via interconnecting busses. Baxter and Applicant's invention cannot be considered to be in the same field of endeavor, simply because both involve the interconnection of multiple

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computers. Indeed, the differences between Baxter and Applicant's invention appear greater than the differences between the memory modules of the *Wang Laboratories* case. In Applicant's claimed invention, an array of computers is integrated in a unitary substrate (e.g., a single silicon chip). Space for components and interconnections is extremely limited and is a primary design concern. Interconnections that cross one another require additional metal layers that increase production cost and decrease production yield. In addition, the capacitance and other electrical characteristics of the interconnections must be designed to facilitate increased switching speeds within the circuits. In contrast, Baxter relates to a network of individual computers mounted on cards that are plugged into the network. (Baxter, Col. 3, Lines 11-19) In Baxter, the computers communicate through an interface 22 that couples the components (microprocessor, memory, and other associated hardware) of the card 20 into busses 24, apparently by plugging the card 20 into a slot or the like, although the exact connection mechanism is not disclosed. Obviously, the design considerations of coupling computers on cards via a buss are quite different than connecting computers embedded in a single integrated circuit chip. Certainly, the differences between Baxter and Applicant's claimed invention are far greater than the differences between the fields of endeavor compared in *Wang Laboratories*.

With respect to the second part of the non-analogous art test, Applicant notes that Baxter and Applicant's invention are directed to very different particular problems. (See e.g., *In re Wang* cited above) The object of Baxter is to provide an algorithm for exchanging information between quadrants of a mesh network, that was not susceptible to node contention and has a relatively high information exchange rate. In Baxter, the exchange of information between nodes is controlled by a controller 26 (Col. 3, Lines 38-53) in order to simultaneously exchange information between sets of nodes (Col. 3, Lines 1-7). In contrast, Applicant's invention is directed to providing flexible, independent communication between adjacent computers of an array.

Because Baxter and Applicant's claimed invention are not from the same field of endeavor, and because Baxter is not directed to the particular problem addressed by Applicant's invention, Baxter is nonanalogous art. Therefore, the rejections under 35 U.S.C. §103 are improper and should be withdrawn.

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Claims 14, 17-21, 23-28 and 43:

Because the combination of Hogenauer and Baxter is improper, the rejections of Claims 14, 17-21, 23-28, and 43 under 35 U.S.C. §103 are improper. Claims 27-28 are canceled. Reconsideration and withdrawal of the rejections of Claims 14, 17-21, 23-26, and 43 is respectfully requested.

Claims 5, 8-11, 15-16, 22, 29, 35, and 44:

Claims 5, 8-11, 15-16, 22, 29, 35, and 44 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hogenauer/Baxter in view of common art. Because the combination of Hogenauer and Baxter is improper, the rejections of Claims 5, 8-11, 15-16, 22, 29, 35, and 44 under 35 U.S.C. §103 are improper. Reconsideration and withdrawal of the rejections of Claims 5, 8-11, 15-16, 22, 29, 35, and 44 is respectfully requested.

Claims 30-33, 36-38, and 42:

Claims 30-33, 36-38, and 42 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hogenauer/Baxter in view of Dokic (US 6,101,598). Because the combination of Hogenauer and Baxter is improper, the rejections of Claims 30-33, 36-38, and 42 under 35 U.S.C. §103 are improper. Reconsideration and withdrawal of the rejections of Claims 30-33, 36-38, and 42 is respectfully requested.

Claim 39:

Claim 39 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hogenauer/Baxter in view of Glass. Claim 39 is canceled.

For the above reasons Applicants request reconsideration and withdrawal of the rejections under 35 U.S.C. § 103.

Examiner Interview:

A telephone interview regarding the merits of the application was held on April 3, 2007. Examiner Brian P. Johnson, attorney Larry E. Henneman, Jr., patent agent Nema Berezny, and attorney F. Eric Saunders participated in the interview.

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Mr. Henneman requested the approval of Examiner Johnson to amend the limitations of Claim 39 into Claim 1 in an after final amendment. Examiner Johnson declined.

Many of the claims were discussed in view of the prior art of record. Examiner Johnson agreed that a claim including the limitations of Claims 1, 7, and 27 would overcome the outstanding rejections. In addition, Examiner Johnson agreed that a claim including the limitations of Claims 1, 7, and 28 would overcome the outstanding rejections.

Applicant has attempted to provide a complete and accurate summary of the interview. If the Examiner disagrees with anything in this interview summary, Applicant welcomes any clarifying comments. Mr. Henneman, Mr. Saunders, and Ms. Berezny express their appreciation to the Examiner for his thoughtful input and spirit of cooperation.

New Claims 45-59:

New Claims 45-49 depend, either directly or indirectly, from Claim 1 and are, therefore distinguishable over the cited prior art for at least the same reasons as Claim 1.

New Claim 50 is a combination of previous Claims 1, 7, and 28, which the Examiner agreed overcomes the outstanding rejections. New Claims 51 and 52 depend from Claim 50 and are distinguished over the prior art of record for at least the same reasons.

New Claim 53 is a combination of previous Claims 1, 7, and 27, which the Examiner agreed overcomes the outstanding rejections. New Claims 54 and 55 depend from Claim 53 and are distinguished over the prior art of record for at least the same reasons.

New Claim 56 is a combination of previously presented elements. Claim 56 is allowable over the prior art of record for at least the same reasons as Claim 1.

New Claim 57 describes the data paths of the invention as physical point-to-point links. An excerpt from Wikipedia, a popular on-line encyclopedia, is attached hereto to demonstrate the well accepted meaning of the phrase "physical point-to-point link." No new matter is added.

New Claims 58-59 each recite "dedicated data lines." Therefore, Claims 58-59 are allowable over the prior art of record for at least the same reasons as Claim 1.



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For the foregoing reasons, Applicants believe Claims 1-26, 29-38, and 40-59 are in condition for allowance. Should the Examiner undertake any action other than allowance of Claims 1-26, 29-38, and 40-59, or if the Examiner has any questions or suggestions for expediting the prosecution of this application, the Examiner is requested to contact Applicant's attorney at (269) 279-8820.

Respectfully submitted,

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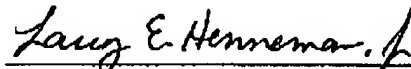
MAY 22 2007

Date: 5/22/07

Larry E. Henneman, Jr., Reg. No. 41,063  
Attorney for Applicant  
Henneman & Associates, PLC  
714 W. Michigan Ave.  
Three Rivers, MI 49093

**CERTIFICATE OF FACSIMILE TRANSMISSION (37 CFR 1.8(a))**

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being transmitted via facsimile, on the date shown below, to: MS: RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, at (571) 273-8300.

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Larry E. Henneman, Jr.